IN THE CLAIMS

Please cancel claims 1-19 without prejudice.

Please add claims 20- 41 as follows:

1.-19. (Cancelled)

20. (New) A method for producing a binary information memory cell comprising:

producing a first electrically conductive region associated with a substrate;

producing an auxiliary structure of a prescribed thickness on the first electrically conductive region;

producing a second electrically conductive region on the auxiliary structure;

removing the auxiliary structure after the second electrically conductive region has been produced, so that a cavity is formed between the first electrically conductive region and the second electrically conductive region, the distance between the first electrically conductive region and the second electrically conductive region corresponding to a tunnel spacing; and

configuring the first and second electrically conductive regions such that upon applying a first voltage to the first and second electrically conductive regions a structure which at least partially bridges the distance between the first and second electrically conductive regions is formed from material from at least one of the electrically conductive regions.

21. (New) The method of claim 20, comprising wherein applying a second voltage to the electrically conductive regions, material from the structure which at least partially bridges the distance between the electrically conductive regions is taken back.

22. (New) The method of claim 20, comprising:

defining the auxiliary structure to be a self-assembled monolayer.

23. (New) The method of claim 20, comprising:

producing the auxiliary structure using an atomic layer deposition method.

24. (New) The method of claim 20, comprising:

producing the auxiliary structure using a molecular beam epitaxy method.

25. (New) The method of claim 20, comprising:

defining the distance between the first conductive region and the second conductive region to be 0.5 nm and 5 nm.

26. (New) The method of claim 20, comprising:

defining the distance between the first conductive region and the second conductive region to be between 0.6 nm and 2 nm.

27. (New) The method of claim 20, comprising:

in which the first electrically conductive region is a first interconnect and the second electrically conductive region is a second interconnect, which interconnects are produced so as to run toward one another at substantially right angles.

28. (New) The method of claim 20, comprising:

defining the substrate to be a silicon substrate.

29. (New) The method of claim 20, comprising:

forming the first electrically conductive region or the second electrically conductive region from at least one material from a group consisting of a solid-state electrolyte, a glass

comprising metal ions, a semiconductor comprising metal ions, or a chalcogenide.

30. (New) The method of claim 20, comprising:

forming the first electrically conductive region or the second electrically conductive region from silver sulfide.

31. (New) The method of claim 20, comprising:

forming the first electrically conductive region or the second electrically conductive region from metal material.

32. (New) The method of claim 20, comprising:

forming the first electrically conductive region or the second electrically conductive region from at least one material from a group consisting of silver, copper, aluminum, gold and/or platinum.

33. (New) A binary information memory cell comprising:

a substrate;

a first electrically conductive region associated with the substrate;

a second electrically conductive region arranged at a prescribable distance from the first electrically conductive region such that a cavity is formed between the first and second electrically conductive regions; and

wherein the first and second electrically conductive regions are set up such that upon application of a first voltage to the electrically conductive regions a structure which at least partially bridges the distance between the electrically conductive regions is formed in freely growing fashion from material from at least one of the electrically conductive regions; and upon application of a second voltage to the electrically conductive regions material from a

structure which at least partially bridges the distance between the electrically conductive regions is taken back.

34. (New) The memory cell of claim 33, comprising wherein the first or the second electrically conductive region is made of metallic material.

35. (New) The memory cell of claim33, comprising wherein the first or the second electrically conductive region is made of at least one material from a group consisting of silver, copper, aluminum, gold and/or platinum.

36. (New) A binary information memory cell arrangement comprising:

a plurality of binary information memory cells having one or more memory cells comprising:

a substrate;

a first electrically conductive region associated with the substrate;

a second electrically conductive region arranged at a prescribable distance from the first electrically conductive region such that a cavity is formed between the first and second electrically conductive regions; and

wherein the first and second electrically conductive regions are set up such that upon application of a first voltage to the electrically conductive regions a structure which at least partially bridges the distance between the electrically conductive regions is formed in freely growing fashion from material from at least one of the electrically conductive regions; and upon application of a second voltage to the electrically conductive regions material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back.

37. (New) The binary information memory cell arrangement of claim 36, comprising

wherein the binary information memory cells are arranged in matrix form.

38. (New) The binary information memory cell arrangement of claim 36, in which selection elements for selecting a binary information memory cell are produced in and/or on the substrate for at least some of the binary information memory cells.

39. (New) The binary information memory cell arrangement as claimed in claim 38, in which the selection elements are field effect transistors.

40. (New) The binary information memory cell arrangement as claimed in claim 39, in which the selection elements are vertical field effect transistors.

41. (New) A binary information memory cell comprising:

a substrate;

a first electrically conductive means associated with the substrate;

a second electrically conductive means arranged at a prescribable distance from the first electrically conductive means such that a cavity is formed between the first and second electrically conductive means; and

wherein the first and second electrically conductive means are set up such that upon application of a first voltage to the electrically conductive means a structure which at least partially bridges the distance between the electrically conductive means is formed in freely growing fashion from material from at least one of the electrically conductive means; and upon application of a second voltage to the electrically conductive means material from a structure which at least partially bridges the distance between the electrically conductive regions is taken back.